

SSD222Q

Smart Display CAM Controller with Embedded 16-bit 256MB DDR3

Preliminary Product Brief

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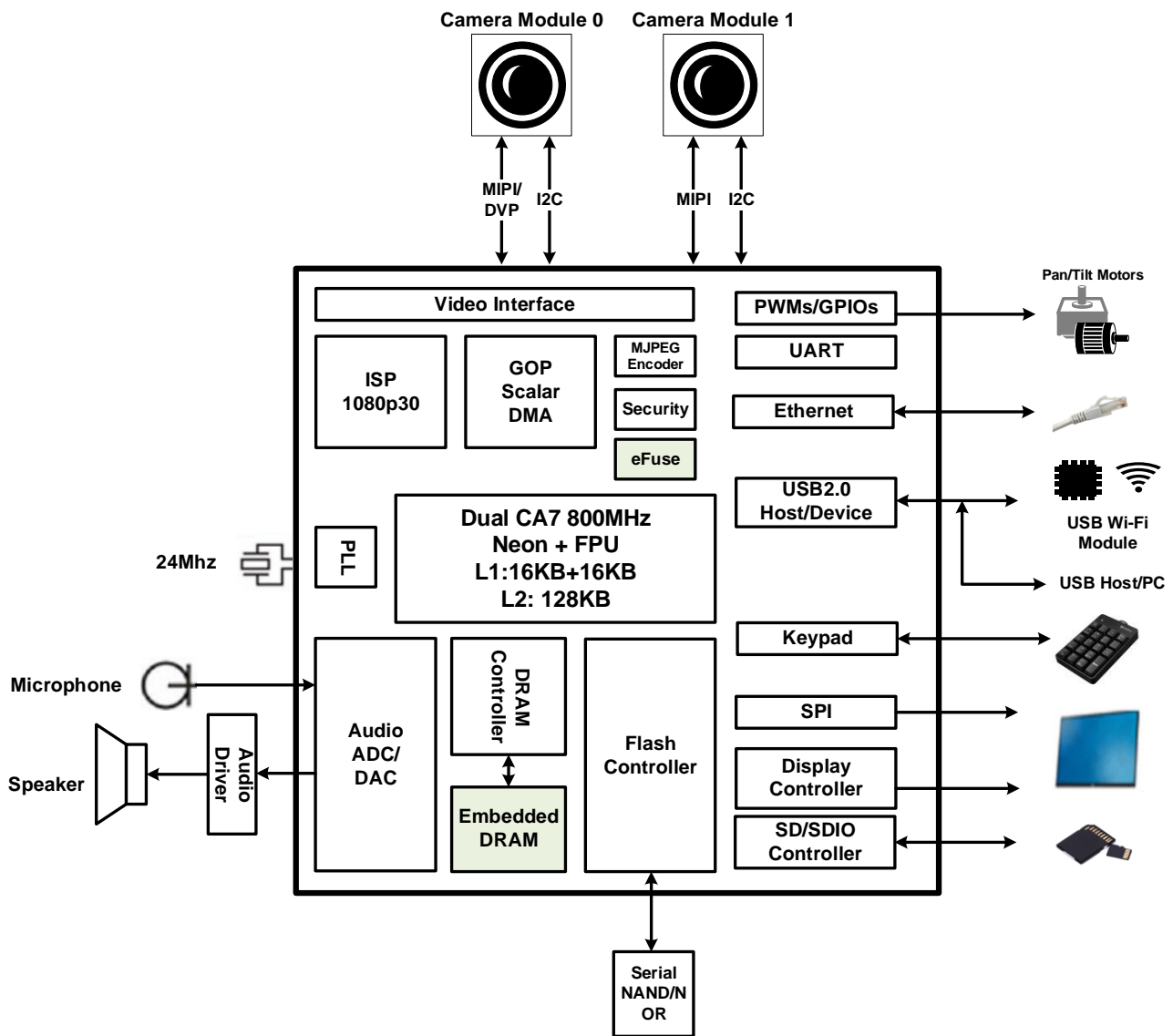
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FEATURES

- **High Performance Processor Core**
 - ARM Cortex-A7 Dual Core up to 1 GHz
 - 16KB I-Cache/16KB D-Cache/128KB L2-Cache
 - Neon and FPU
 - Memory Management Unit for Linux support
 - DMA Engine
- **Image/Video Processor**
 - Supports 8/10-bit parallel interface for raw data input
 - Supports max. two MIPI interfaces with 2 or 1 data lane and 2 clock lanes, up to 1.5GHz
 - Supports 8/10-bit BT.601/656 parallel interface
 - ISP processing performance up to 1920x1080p30
 - Bad pixel compensation
 - Temporal-domain Noise Reduction (3DNR)
 - Bayer domain Spatial-domain Noise Reduction (2DNR)
 - Bayer domain filter to remove purple false color in highlight regions
 - Optical black correction
 - Lens shading compensation
 - Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
 - CFA color interpolation
 - Color correction
 - Gamma correction
 - Video stabilization
 - Frame buffer data compression and de-compression to save memory bandwidth
 - Wide Dynamic Range (WDR) with local tone mapping
- **JPEG Encoder**
 - Supports JPEG baseline encoding
 - Supports YUV422 or YUV420 formats
 - Supports max. resolution 720p (1280x720) with 30fps
- **Display Subsystem**
 - Built-in contrast, brightness, sharpness, and saturation, 3D NR, Gamma control
- TTL output up to 1280x800 60fps with RGB565 or RGB666 or RGB888 format
- BT.656 output up to 720p60
- Serial RGB up to 800x600 60fps
- Supports SPI panel, clock frequency up to 54MHz
- Supports FHD graphic layer with Index 4/8, ARGB1555/ARGB4444/ARGB8888, and RGB565 format
- Supports UI/OSD layer with max. resolution 1280x800
- **2D Graphics Engine**
 - Line draw
 - Rectangle/gradient rectangle fill
 - Bitblt/Stretch Bitblt/Italic Bitblt
 - Palette mode (1/2/4/8-bit)
 - Format transformation
 - Color space conversion
 - Clipping
 - Alpha blending
 - Rotation/Mirror
 - Dither
- **Audio Processor**
 - Three mono ADCs or one mono + one stereo ADC for microphone input
 - Two stereo DMIC inputs
 - I2S TDM 8-channel, RX 2/4/8 channels, TX 2 channels
 - One stereo DAC for lineout
 - One HP Driver headphone set
 - I2S supports 8K/16K/32K/48K/96KHz sampling rate audio recording
 - ADC Pre-Amp gain supports 0dB, 6dB, 13dB, 23dB, 30dB, and 36dB
 - ADC boost gain supports -6dB ~ 15dB or 0dB ~ 21dB with interval 3dB
 - ADC digital gain supports -63.5dB ~ 33dB with interval 0.5dB, can be muted to zero
 - SNR of DR A-Weighted ADC > 90dB (@gain = 0dB)

- **NOR/NAND Flash Interface**
 - Supports 1/2/4-bit SPI-NOR / NAND flash with two chip selects
- **SDIO 2.0 Interface**
 - Compatible with SDIO spec. 2.0, data bus 1/4 bit mode
 - Compatible with SD spec. 2.0, data bus 1/4 bit mode
- **USB 2.0 Interface**
 - One USB2.0 configurable host and device
 - Host mode supports EHCI specification
 - Device mode supports 4 end points
- **DRAM Memory**
 - Embedded 16-bit 256MB DDR3 memory with max. 1866Mbps
 - Supports auto-refresh and self-refresh mode
- **Ethernet**
 - Supports one Ethernet port
 - Supports 10/100Mbps half/full-duplex
 - One built-in 10/100M Ethernet PHY
 - Supports one RMI1 to connect external PHY
 - Supports two LEDs for ePHY
- **Security Engines**
 - Supports AES/DES/3DES/RSA/SHA-1/SHA-256
 - Supports secure booting
- **Boot options**
 - ROM
 - SPI NOR
 - SPI NAND with ECC
 - SD Card and USB
- **Peripherals**
 - Dedicated GPIOs for system control
 - Four PWM outputs
 - Three generic UARTs and one fast UART with flow control
 - Three generic timers and one watchdog timer
 - Two SPI masters
 - Two I2C masters
 - Keypad supports up to 7x7, single mode
- **Miscellaneous**
 - Built-in eFuse with 1024-bit to store device ID, AES key, chip configurations, etc.
 - Built-in power on reset (POR)
 - Built-in SAR ADC with 2-channel analog inputs for different kinds of applications
- **Operating Voltage Range**
 - Core: 0.9V
 - I/O: 1.8V/3.3V
 - DRAM: 1.5V (DDR3)
 - Power Consumption: TBD.
 - Ambient Temperature -20°C ~ 85°C
- **Package**
 - 128-pin QFN, 12.3mm x 12.3mm
 - Moisture Sensitivity Level (MSL): 3

BLOCK DIAGRAM



GENERAL DESCRIPTION

The SSD222Q is a highly integrated SOC product for face access and smart display applications.

Based on ARM Cortex-A7 dual-core, the SSD222Q integrates image sensor interface, advanced ISP, high performance JPEG encoder, 2D graphics engine, TTL/serial RGB display with adjustable picture quality engine and other useful peripherals.

A typical utilization of the SSD222Q application processor is demonstrated in the block diagram. The completed system includes NOR/NAND flash, DRAM, SD card, and USB port, and diversified audio connection. Before output to the panel, the images can be enhanced with respect to brightness/contrast/saturation/sharpness to give the best picture quality.

The NOR or NAND flash is usually reserved for operating system and application software. Moreover, other peripherals like SAR ADC, Audio ADC/DAC, UARTs, PWMs, GPIOs and SPI are supported to realize applications with maximal flexibility.

The SSD222Q supports secure booting and personalization authentication mechanism for securing system. The AES/DES/3DES cipher engines could also help encrypt the compressed video/audio streams for privacy protection.

The SSD222Q, powered by SigmaStar Technology, comes with a complete hardware platform and software SDK, allowing customers to speed up "Time-to-Market."