# SSD201
# Smart HD Display Controller

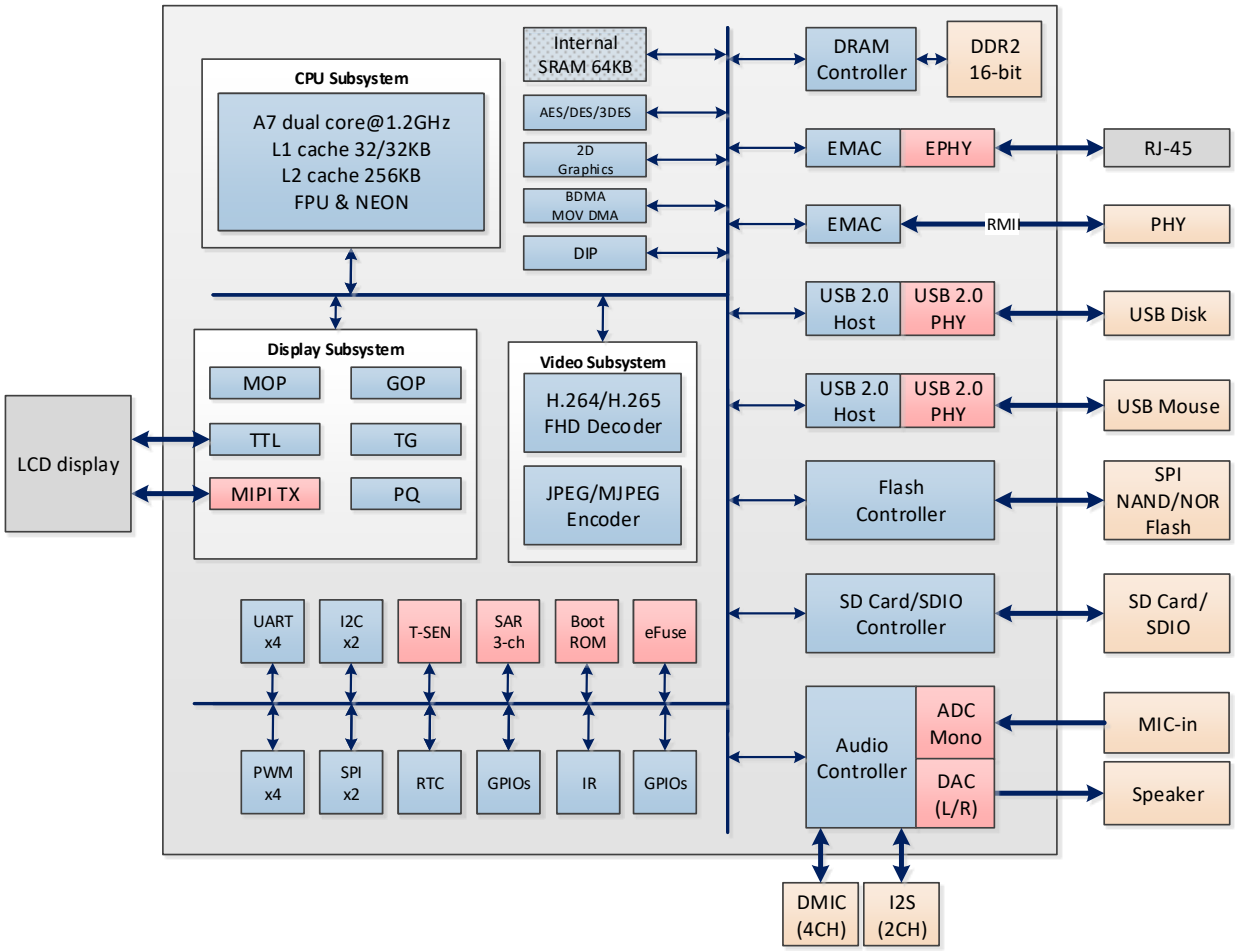
**Preliminary Product Brief**

# FEATURES

- High Performance Processor Core
  - ARM Cortex-A7 Dual Core up to 1.2GHz
  - 32KB I-Cache/32KB D-Cache/256KB L2-Cache
  - Neon and FPU
  - Memory Management Unit for Linux support
  - DMA Engine
- H.264/AVC Decoder
  - Variable block size (16x16, 16x8, 8x16, 8x8, 8x4, 4x8 and 4x4)
  - CABAC/CAVLC support
  - Error detection, concealment and error resilience tools
  - Supports max. resolution FHD (1920x1080) with 60fps decode
- H.265/HEVC Decoder
  - I/P/B slices
    - All intra-prediction modes
    - All inter-prediction modes
  - Variable CTU size: 64x64 to 16x16
    - Variable Prediction Unit (PU) size: 64x64 to 4x4
    - Variable Transform Unit (TU) size: 32x32 to 4x4
  - High performance CABAC decoding
  - Sample Adaptive Offset (SAO)
  - Robust error concealment
  - Supports max. resolution FHD (1920x1080) with 60fps decode
- JPEG Encoder
  - Supports JPEG baseline encoding
  - Supports YUV422 or YUV420 formats
  - Supports max. resolution FHD (1920x1080) with 15fps
- Display Subsystem
  - Supports multi-window (max. 4 + 1 PIP) fetch, merge, and scale-up function
  - Built-in contrast, brightness, sharpness, and saturation control
  - TTL output up to HD 60fps with RGB565 or RGB666 or RGB888 format
  - MIPI TX DSI 4-lane with max. 1.5Gbps and output up to FHD 60fps
  - Supports FHD graphic layer with Index 4/8, ARGB1555/ARGB4444/ARGB8888, RGB565, and YUV422 format
  - Supports UI/OSD layer with max. resolution FHD (1920x1080)
  - Supports cursor layer with max. resolution 256x256
- 2D Graphics Engine
  - Line draw
  - Rectangle/gradient rectangle fill
  - Bitblt/Stretch Bitblt/Italic Bitblt
  - Palette mode (1/2/4/8-bit)
  - Format transformation
  - Color space conversion
  - Clipping
  - Alpha blending
  - Rotation/Mirror
  - Dither
- Audio Processor
  - One mono ADC for microphone input
  - Two stereo DMIC inputs
  - Two-channel I2S digital audio input and output
  - One stereo DAC for lineout
  - Supports 8K/16K/32K/48KHz sampling rate audio recording
  - ADC Pre-Amp gain supports 0dB, 6dB, 13dB, 23dB, 30dB, and 36dB
  - ADC boost gain supports -6dB ~ 15dB or 0dB ~ 21dB with interval 3dB
  - ADC digital gain supports -63.5dB ~ 33dB with interval 0.5dB, can be muted to zero
  - SNR of DR A-Weighted ADC > 90dB (@gain = 0dB)
- NOR/NAND Flash Interface
  - Supports 1/2/4-bit SPI-NOR / NAND (with ECC) flash with two chip selects

- SDIO 2.0 Interface
  - Compatible with SDIO spec. 2.0, data bus 1/4 bit mode
  - Compatible with SD spec. 2.0, data bus 1/4 bit modeUSB 2.0 Interface
  - Two high-speed USB2.0 hosts
  - Connects to external mouse, Wi-Fi, AI chip or hard disk
- DRAM Memory
  - Supports 16-bit 512Mb DDR2 memory with max. 1333Mbps
  - One embedded DDR2 memory
  - Supports ODT function
  - Supports auto-refresh and self-refresh mode
- Ethernet
  - Supports two Ethernet ports
  - Supports 10/100Mbps half/full-duplex
  - One built-in 10/100M Ethernet PHY
  - Supports one RMII to connect external PHY
  - Supports two LEDs for ePHY
- Security Engines
  - Supports AES/DES/3DES/RSA/SHA-I/SHA-256
  - Supports secure booting
- Real Time Clock (RTC)
  - Built-in RTC working with 32.768 KHz crystal
  - Tick time interrupt (millisecond)
  - Supports ultra-low power (<3uA) RTC-mode for long battery application
- Peripherals
  - Dedicated GPIOs for system control
  - Four PWM outputs
  - Three generic UARTs and one fast UART with flow control
  - Three generic timers and one watchdog timer
  - One SPI master
  - Two I2C masters
  - One IR input
- Miscellaneous
  - Built-in efuse with 1024-bit to store device ID, AES key, chip configurations, etc.
  - Built-in power on reset (POR)
  - Built-in SAR ADC with 3-channel analog inputs for different kinds of applications
- Operating Voltage Range
  - Core: 0.9V
  - I/O: 1.8V ~ 3.3V
  - DRAM: 1.8V
  - Power Consumption: TBD.
  - Operation temperature -20°C ~ 85°C
- Package
  - 128-pin QFN, 12.3mm x 12.3mm
  - Moisture Sensitivity Level: 3

# BLOCK DIAGRAM



# GENERAL DESCRIPTION

The SSD201 is a highly integrated SOC. Based on ARM Cortex-A7 dual-core, it integrates H.264/H.265 video decoder, 2D graphics engine, TTL/MIPI display with adjustable picture quality engine and other useful peripherals for smart display applications.

A typical utilization of the SSD201 application processor is demonstrated in the block diagram. The completed system includes a connectivity module (Wi-Fi or Ethernet), and a non-volatile storage (NOR flash, NAND flash or SD card). External crystal of 32KHz frequency is used to drive the Real Time Clock (RTC), which can keep time scale when the main system clock is off. The H.264/H.265 engine decodes video streams from network and sends them to the display sub-system. Before outputting to TTL or MIPI TX panel, the images can be enhanced with respect to brightness/contrast/saturation/sharpness to give the best picture quality. The NOR or NAND flash is usually reserved for operating system and application software. Moreover, other peripherals like SAR ADC, Audio ADC/DAC, UARTs, PWMs, GPIOs and SPI are supported to realize applications with maximal flexibility.

Besides, the SSD201 supports secure booting and personalization authentication mechanism for securing system. The AES/DES/3DES cipher engines could also help encrypt the compressed video/audio streams to protect privacy.