SSD210
Smart Display CAM Controller

Preliminary Product Brief Version 0.6

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REVISION HISTORY

Revision No.	Description	Date
0.1	• Initial release	10/15/2020
0.2	• Removed Ethernet support	12/28/2020
0.3	• Updated Signal Description by adding Power Domain information • Updated ambient operation temperature range • Added Minimum Order Quantity and Moisture Sensitivity Level	01/21/2021
0.4	• Added Hardware Power Sequence Procedure and MSPI Operation Example	02/26/2021
0.5	• Added MIPI sensor support	08/05/2021
0.6	• Added Thermal Resistance data	12/14/2021

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FEATURES

- High Performance Processor Core
  - ARM Cortex-A7 Dual Core up to 1 GHz
  - 16KB I-Cache/16KB D-Cache/128KB L2-Cache
  - Neon and FPU
  - Memory Management Unit for Linux support
  - DMA Engine
- Image/Video Processor
  - Supports max. two MIPI interfaces with 2 or 1 data lane and 2 clock lanes, up to 1.5GHz
  - Supports 8-bit BT.656 parallel interface
  - ISP processing performance up to 1920x1080p30
  - Bad pixel compensation
  - Temporal-domain Noise Reduction (3DNR)
  - Bayer domain Spatial-domain Noise Reduction (2DNR)
  - Bayer domain filter to remove purple false color in highlight regions
  - Optical black correction
  - Lens shading compensation
  - Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
  - CFA color interpolation
  - Color correction
  - Gamma correction
  - Video stabilization
  - Frame buffer data compression and de-compression to save memory bandwidth
  - Wide Dynamic Range (WDR) with local tone mapping
- JPEG Encoder
  - Supports JPEG baseline encoding
  - Supports YUV422 or YUV420 formats
  - Supports max. resolution 720p (1280x720) with 30fps
- Display Subsystem
  - Built-in contrast, brightness, sharpness, and saturation, 3D NR, Gamma control
  - TTL output up to 1280x800 60fps with RGB565 or RGB666 format
  - BT.656 output up to 720p60
  - Serial RGB up to 800x600 60fps
  - Supports SPI panel, clock frequency up to 54MHz
  - Supports FHD graphic layer with Index 4/8, ARGB1555/ARGB4444/ARGB8888, and RGB565 format
  - Supports UI/OSD layer with max. resolution 1280x800
- 2D Graphics Engine
  - Line draw
  - Rectangle/gradient rectangle fill
  - Bitblt/Stretch Bitblt/Italic Bitblt
  - Palette mode (1/2/4/8-bit)
  - Format transformation
  - Color space conversion
  - Clipping
  - Alpha blending
  - Rotation/Mirror
  - Dither
- Audio Processor
  - Two stereo DMIC inputs
  - I2S TDM 8-channel, RX 2/4/8 channels, TX 2 channels
  - One mono DAC for lineout
  - I2S supports 8K/16K/32K/48K/96KHz sampling rate audio recording
- NOR/NAND Flash Interface
  - Embedded 1/2/4-bit SPI-NOR / NAND flash with two chip selects
- SDIO 2.0 Interface
  - Compatible with SDIO spec. 2.0, data bus 1/4 bit mode
  - Compatible with SD spec. 2.0, data bus 1/4 bit mode
- USB 2.0 Interface
  - One USB2.0 configurable host and device
    - Host mode supports EHCI specification
    - Device mode supports 4 end points

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- DRAM Memory
  - Supports 16-bit 64MB DDR2 memory with max. 1333Mbps
  - Supports auto-refresh and self-refresh mode
- Security Engines
  - Supports AES/DES/3DES/RSA/SHA-I/SHA-256
  - Supports secure booting
- Boot options
  - ROM
  - SPI NOR
  - SPI NAND with ECC
  - USB
- Peripherals
  - Dedicated GPIOs for system control
  - Four PWM outputs
  - Three generic UARTs and one fast UART with flow control
  - Three generic timers and one watchdog timer
  - Two SPI masters
  - Two I2C masters
- Miscellaneous
  - Built-in eFuse with 1024-bit to store device ID, AES key, chip configurations, etc.
  - Built-in power on reset (POR)
  - Built-in SAR ADC with 3-channel analog inputs for different kinds of applications
- Operating Voltage Range
  - Core: 0.9V
  - I/O: 1.8V ~ 3.3V
  - DRAM: 1.8V (DDR2)
  - Power Consumption: TBD.
  - Operation temperature -20°C ~ 85°C
- Package
  - 68-pin QFN, 7mm x 7mm
  - Moisture Sensitivity Level: 3

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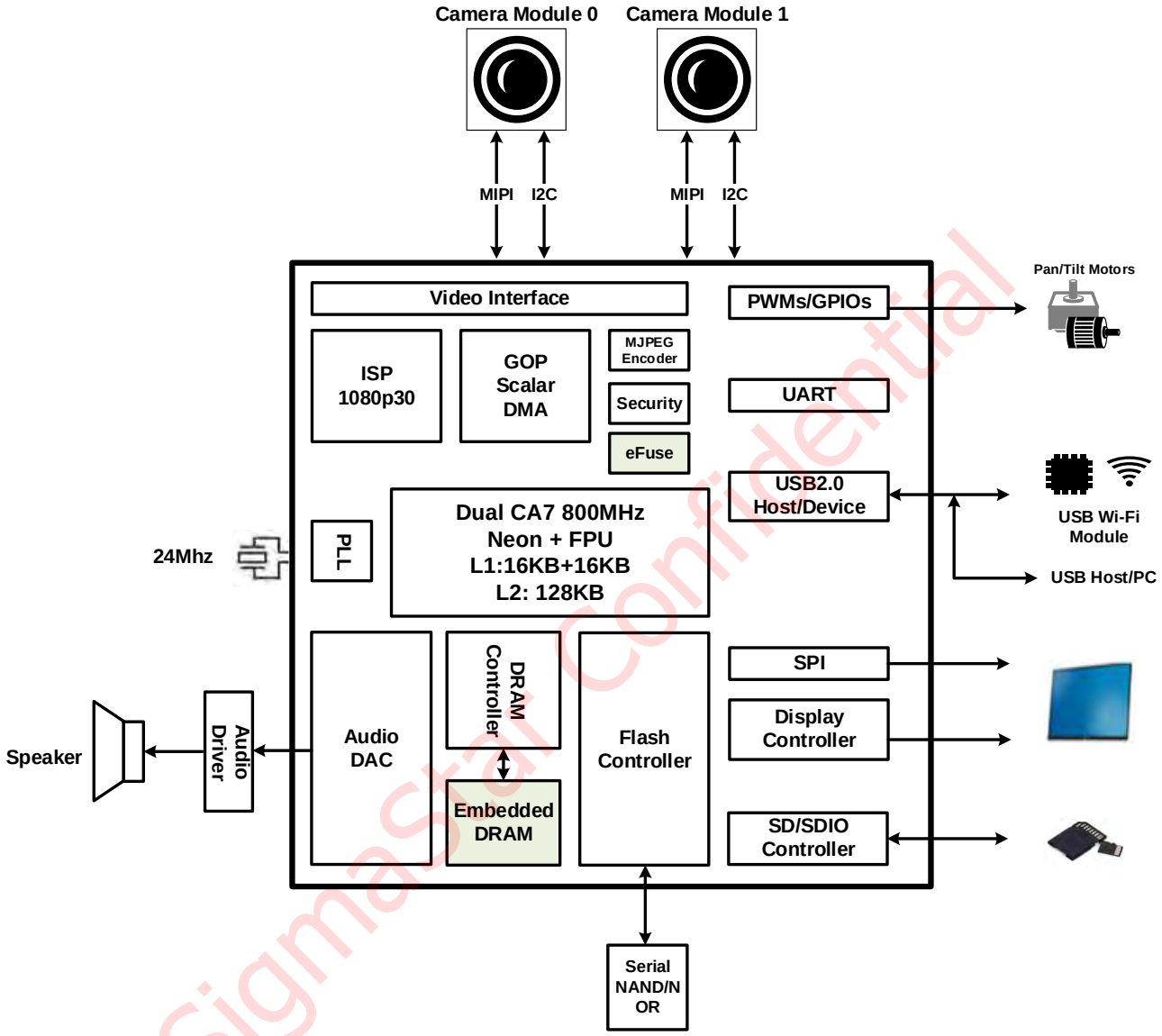
BLOCK DIAGRAM



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GENERAL DESCRIPTION

The SSD210 is a highly integrated SOC product for face access and smart display applications.

Based on ARM Cortex-A7 dual-core, the SSD210 integrates image sensor interface, advanced ISP, high performance JPEG encoder, 2D graphics engine, TTL/serial RGB display with adjustable picture quality engine and other useful peripherals.

A typical utilization of the SSD210 application processor is demonstrated in the block diagram. The completed system includes NOR/NAND flash, DRAM, SD card, and USB port, and diversified audio connection. Before output to the panel, the images can be enhanced with respect to brightness/contrast/saturation/sharpness to give the best picture quality.

The NOR or NAND flash is usually reserved for operating system and application software. Moreover, other peripherals like SAR ADC, Audio DAC, UARTs, PWMs, GPIOs and SPI are supported to realize applications with maximal flexibility.

The SSD210 supports secure booting and personalization authentication mechanism for securing system. The AES/DES/3DES cipher engines could also help encrypt the compressed video/audio streams for privacy protection.

The SSD210, powered by SigmaStar Technology, comes with a complete hardware platform and software SDK, allowing customers to speed up "Time-to-Market."

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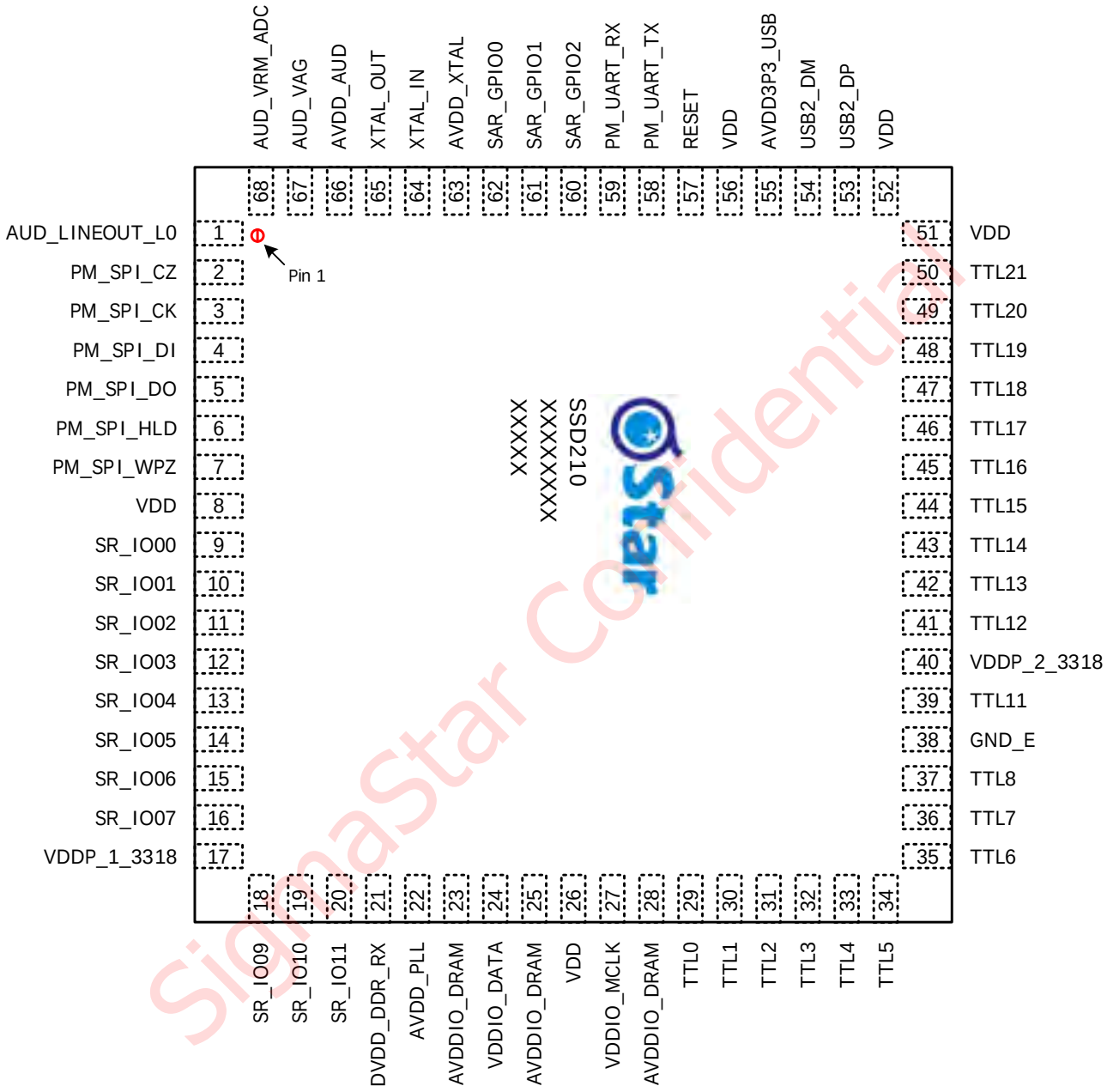
PIN DIAGRAM



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SIGNAL DESCRIPTION

Signal Name	Signal Type	Function	Power Domain	Pin Location
System Reset Interface				
RESET	I	System Reset (Active High)	AVDD_XTAL	57
Debug UART Interface				
PM_UART_RX	I	Debug UART Receive Data Input with Pull Up Resistor / Slave I2C Serial Clock	AVDD_XTAL	59
PM_UART_TX	O	Debug UART Transmit Data Output with Pull Up Resistor / Slave I2C Serial Data	AVDD_XTAL	58
System Interface				
XTAL_IN	I	24MHz Crystal Input	AVDD_XTAL	64
XTAL_OUT	O	24MHz Crystal Output	AVDD_XTAL	65
SPI Flash Interface				
PM_SPI_CZ	O	SPI Flash Chip Select (Active Low)	AVDD_XTAL	2
PM_SPI_CK	O	SPI Flash Clock	AVDD_XTAL	3
PM_SPI_DI	O	SPI Flash Serial Data To Device (MOSI)	AVDD_XTAL	4
PM_SPI_DO	I	SPI Flash Serial Data From Device (MISO)	AVDD_XTAL	5
PM_SPI_WPZ	O	SPI Flash Write Protect	AVDD_XTAL	7
PM_SPI_HLD	O	SPI Flash Hold	AVDD_XTAL	6
SAR_GPIO0	I	General Purpose Input/Output or Muxed to SARADC Input Channel 0	AVDD_XTAL	62
SAR_GPIO1	I	General Purpose Input/Output or Muxed to SARADC Input Channel 1	AVDD_XTAL	61
SAR_GPIO2	I	General Purpose Input/Output or Muxed to SARADC Input Channel 2	AVDD_XTAL	60
Image Sensor Interface				
SR_IO00	I/O	Sensor General Purpose Input/Output 0	VDDP_1_3318	9
SR_IO01	I/O	Sensor General Purpose Input/Output 1	VDDP_1_3318	10
SR_IO02	I/O	Sensor General Purpose Input/Output 2	VDDP_1_3318	11
SR_IO03	I/O	Sensor General Purpose Input/Output 3	VDDP_1_3318	12
SR_IO04	I/O	Sensor General Purpose Input/Output 4	VDDP_1_3318	13
SR_IO05	I/O	Sensor General Purpose Input/Output 5	VDDP_1_3318	14
SR_IO06	I/O	Sensor General Purpose Input/Output 6	VDDP_1_3318	15

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Signal Name	Signal Type	Function	Power Domain	Pin Location
SR_IO07	I/O	Sensor General Purpose Input/Output 7	VDDP_1_3318	16
SR_IO09	I/O	Sensor General Purpose Input/Output 9	VDDP_1_3318	18
SR_IO10	I/O	Sensor General Purpose Input/Output 10	VDDP_1_3318	19
SR_IO11	I/O	Sensor General Purpose Input/Output 11	VDDP_1_3318	20
TTL Interface				
TTL0	I/O	Parallel LCDGeneral Purpose Input/Output 0	VDDP_2_3318	29
TTL1	I/O	Parallel LCDGeneral Purpose Input/Output 1	VDDP_2_3318	30
TTL2	I/O	Parallel LCDGeneral Purpose Input/Output 2	VDDP_2_3318	31
TTL3	I/O	Parallel LCDGeneral Purpose Input/Output 3	VDDP_2_3318	32
TTL4	I/O	Parallel LCDGeneral Purpose Input/Output 4	VDDP_2_3318	33
TTL5	I/O	Parallel LCDGeneral Purpose Input/Output 5	VDDP_2_3318	34
TTL6	I/O	Parallel LCDGeneral Purpose Input/Output 6	VDDP_2_3318	35
TTL7	I/O	Parallel LCDGeneral Purpose Input/Output 7	VDDP_2_3318	36
TTL8	I/O	Parallel LCDGeneral Purpose Input/Output 8	VDDP_2_3318	37
TTL11	I/O	Parallel LCDGeneral Purpose Input/Output 11	VDDP_2_3318	39
TTL12	I/O	Parallel LCDGeneral Purpose Input/Output 12	VDDP_2_3318	41
TTL13	I/O	Parallel LCDGeneral Purpose Input/Output 13	VDDP_2_3318	42
TTL14	I/O	Parallel LCDGeneral Purpose Input/Output 14	VDDP_2_3318	43
TTL15	I/O	Parallel LCDGeneral Purpose Input/Output 15	VDDP_2_3318	44
TTL16	I/O	Parallel LCDGeneral Purpose Input/Output 16	VDDP_2_3318	45
TTL17	I/O	Parallel LCDGeneral Purpose Input/Output 17	VDDP_2_3318	46
TTL18	I/O	Parallel LCDGeneral Purpose Input/Output 18	VDDP_2_3318	47
TTL19	I/O	Parallel LCDGeneral Purpose Input/Output 19	VDDP_2_3318	48
TTL20	I/O	Parallel LCDGeneral Purpose Input/Output 20	VDDP_2_3318	49
TTL21	I/O	Parallel LCDGeneral Purpose Input/Output 21	VDDP_2_3318	50

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Signal Name	Signal Type	Function	Power Domain	Pin Location
Audio Line Out Interface				
AUD_LINEOUT_L0	O	Audio Left Channel Line Output	AVDD_AUD	1
AUD_VAG	O	Audio Reference Voltage from 1/2 AVDD_AUD	AVDD_AUD	67
AUD_VRM_ADC	I	Audio Reference Voltage for ADC	AVDD_AUD	68
USB 2.0 Interface				
USB2_DM	I/O	USB 2.0 Differential Pair, Negative	AVDD3P3_USB	54
USB2_DP	I/O	USB 2.0 Differential Pair, Positive	AVDD3P3_USB	53
Power pins				
VDD	Core Power	Digital Core Power		8, 26, 51, 52, 56
DVDD_DDR_RX	Core Power	Digital Power for DDR RX LDO (0.1uF CAP to GND)		21
VDDIO_DATA	DDR Power	IO Power for DDR Data		24
VDDIO_MCLK	DDR Power	IO Power for DDR Clock		27
AVDDIO_DRAM	DDR Power	IO Power for embedded DRAM		23, 25, 28
VDDP_1_3318	1.8V/3.3V Power	Digital Input/Output Power for Domain 1		17
VDDP_2_3318	1.8V/3.3V Power	Digital Input/Output Power for Domain 2		40
AVDD_PLL	3.3V Power	Analog Power for PLL		22
AVDD_XTAL	3.3V Power	Analog Power for XTAL		63
AVDD3P3_USB	3.3V Power	Analog Power for USB2.0		55
AVDD_AUD	3.3V Power	Analog Power for Audio		66
GND_E	GND	Ground		38

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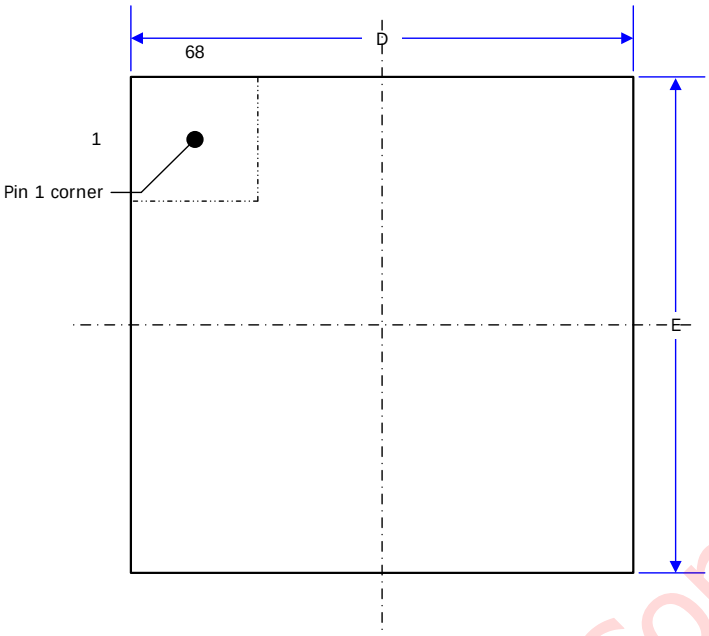
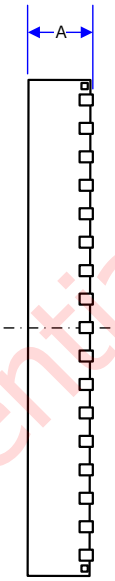
MECHANICAL DIMENSIONS

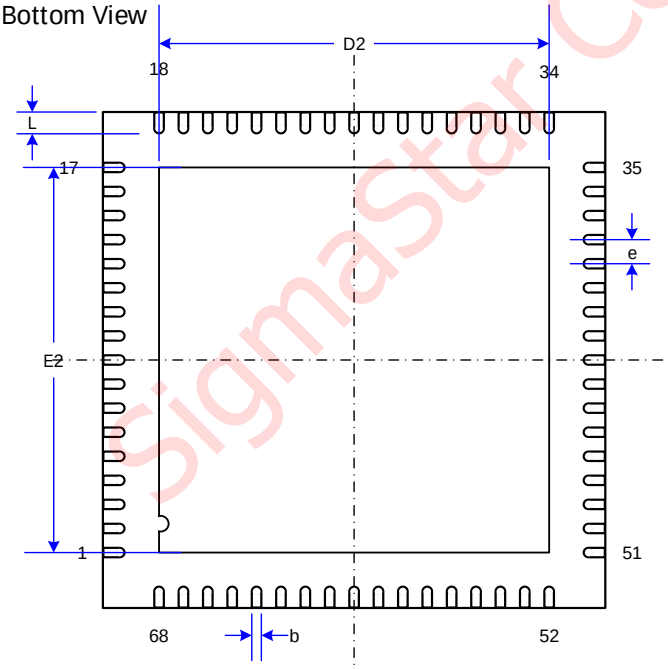
Top View



Side View



Bottom View



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.85	0.90	0.031	0.033	0.035
D	6.90	7.00	7.10	0.272	0.276	0.280
E	6.90	7.00	7.10	0.272	0.276	0.280
D2	5.50	5.60	5.70	0.217	0.220	0.224
E2	5.50	5.60	5.70	0.217	0.220	0.224
b	0.13	0.18	0.23	0.005	0.007	0.009
e	--	0.35	--	--	0.014	--
L	0.30	0.40	0.50	0.012	0.016	0.020

Note: E-pad has to connect to system GND net.

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ELECTRICAL SPECIFICATIONS

Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIGITAL INPUTS					
Input Voltage, High	V_{IH}	VDDP*0.7[Note]			V
Input Voltage, Low	V_{IL}			0.8	V
Input Current, High	I_{IH}			-1.0	uA
Input Current, Low	I_{IL}			1.0	uA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Output Voltage, High	V_{OH}	VDDP-0.1[Note]			V
Output Voltage, Low	V_{OL}			0.1	V
SAR ADC Input		0		V_{VDD_33}	V
AUDIO OUTPUTS					
Line-Out			2.54		Vp-p
XTAL Specifications					
Input Voltage, High	V_{IH}	2.0		3.6	V
Input Voltage, Low	V_{IL}	-0.3		0.8	V
Clock frequency			24		MHz
Crystal accuracy			+/-30		ppm
Long-term jitter			+/-500		ps

Note: VDDP typical voltage is 3.3V or 1.8V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}	3.14	3.3	3.46	V
1.8V Supply Voltage (DDR II)	V_{VDD_18}	1.71	1.8	1.89	V
Core Power Supply Voltage (Core)	V_{VDD_core}	0.87	0.9	0.93	V
Ambient Operation Temperature	T_A	-20		85	°C
Junction Temperature	T_J			125	°C

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max.	Unit
3.3V Supply Voltage	V_{VDD_33}	2.97	3.3	3.63	V
1.8V Supply Voltage (DDR II)	V_{VDD_18}			1.98	V
Core Power Supply Voltage (Core)	V_{VDD_core}			1.1	V
Storage Temperature	T_{STG}	-40		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

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HARDWARE POWER SEQUENCE PROCEDURE

The timing requirements of the hardware reset signal are shown as below:

Hardware Reset

HWRESET: Chip Reset; High Reset (Level)

The HWRESET pin is suggested to connect with 3.3V standby as shown in Figure 1. The VIH is 2V (Typ) +/- 10% (2.2V~1.8V); the VIL is 1.2V (Typ) +/- 10% (1.08V~1.32V). The power sequence is as shown in Figure 2.

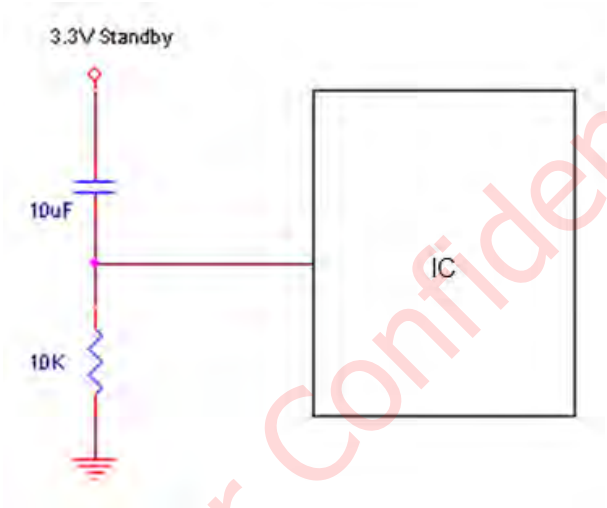

Figure 1: Reset Application Circuit

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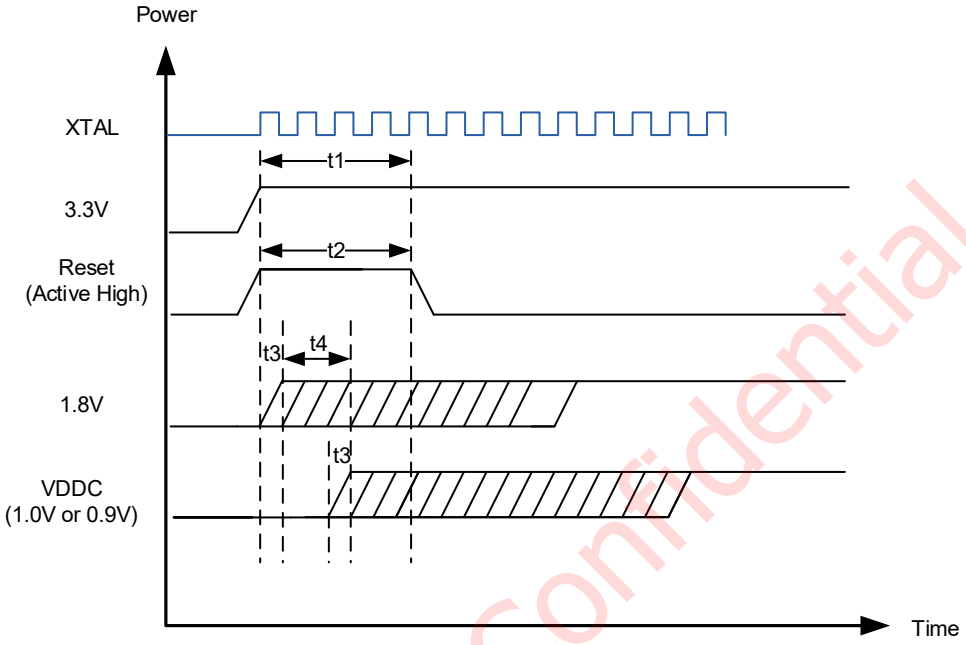
External Reset IC with External LDO

The timing is shown as Figure 2. The RST and power waveform must satisfy Figure 2 with parameters listed in Table 1.



Note:

*3.3V (AVDD_XTAL, AVDD_ETH, AVDD3P3_USB, AVDD_PLL, AVDD_AUD, VDDP_1_3318 (if 3.3V is used), VDDP_2_3318 (if 3.3V is used))

*1.0V/0.9V (VDD)

*1.8V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD, VDDIO_MCLK, VDDP_1_3318 (if 1.8V is used), VDDP_2_3318 (if 1.8V is used))

Figure 2: Power on Sequence

Table 1: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	XTAL stable to Reset falling	5	—	—	ms
t_2	Reset pulse width	5	—	—	ms
t_3	Normal 3.3V, 1.8V, and VDDC power rising time (0% to 100%)	—	—	20	ms
t_4	Normal 3.3V and 1.8V to VDDC lead time	1	—	—	ms

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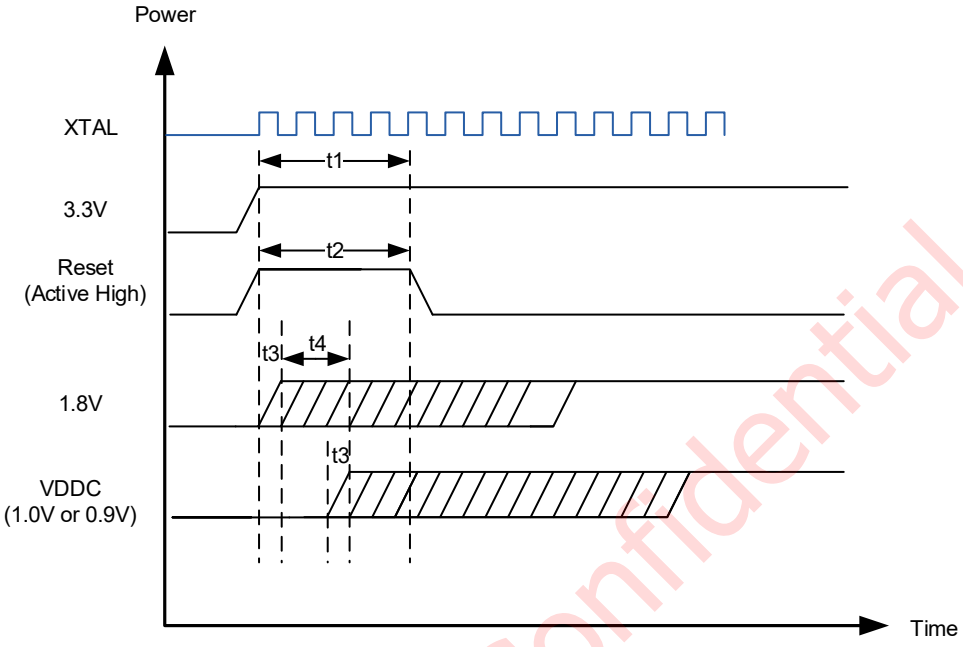
Without External Reset IC with External LDO

The timing is shown as Figure 3. The power waveform must satisfy Figure 3 with parameters listed in Table 2.



Note:

*3.3V (AVDD_XTAL, AVDD_ETH, AVDD3P3_USB, AVDD_PLL, AVDD_AUD, VDDP_1_3318 (if 3.3V is used), VDDP_2_3318 (if 3.3V is used))

*1.0V/0.9V (VDD)

*1.8V (AVDDIO_DRAM, VDDIO_DATA, VDDIO_CMD, VDDIO_MCLK, VDDP_1_3318 (if 1.8V is used), VDDP_2_3318 (if 1.8V is used))

Figure 3: Power on Sequence

Table 2: Power Requirements

Time	Description	Min	Typ.	Max	Unit
t_1	Normal 3.3V, 1.8V, and VDDC power rising time (0% to 100%)	—	—	20	ms
t_2	Normal 3.3V and 1.8V to VDDC lead time	1	—	—	ms

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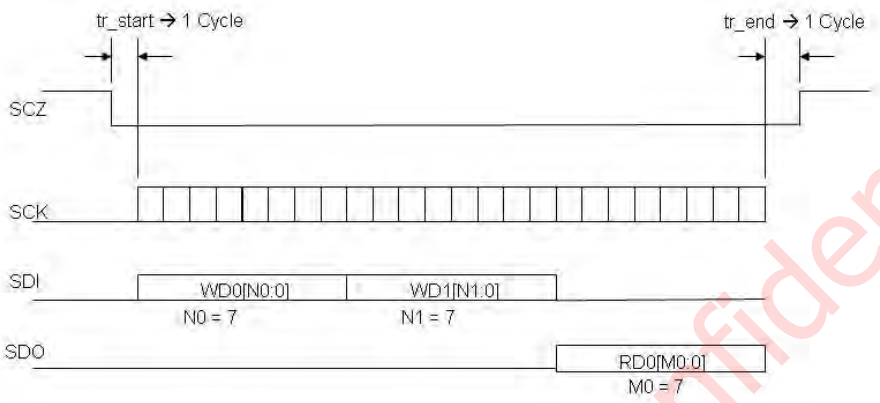
MSPI OPERATION EXAMPLE

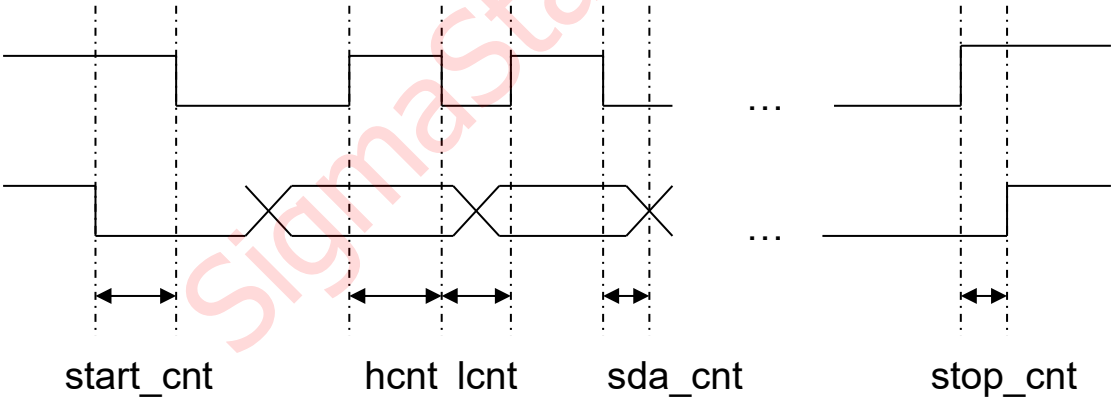
This section describes an example of MSPI operation.

(0) Initialize
(1) CS goes low
(2) Write 2-Byte data
(3) Read 1-Byte data
(4) CS goes high



I2C clock frequency is configurable between 100KHz and 400KHz.

Set MIIC Speed



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clk_miic	12MHz	24MHz
lcnt (>1.3us)	>16T	>31T
hcnt (>0.6us)	>8T	>15T
start (>0.6us)	>8T	>15T
stop (>0.6us)	>8T	>15T
between start and stop (>1.3us)	>16T	>31T
data_latch (>0us)	>0T	>0T
sda change (<0.9us)	<11T	<22T

Register Name	Address	Description
reg_stop_cnt	'h08[15:0]	Sets the SCL and SDA count for stop
reg_hcnt	'h09[15:0]	Sets the SCL clock high-period count
reg_lcnt	'h0a[15:0]	Sets the SCL clock low-period count
reg_sda_cnt	'h0b[15:0]	Sets the clock count between falling edge SCL and SDA
reg_start_cnt	'h0c[15:0]	Sets the SCL and SDA count for start
reg_data_lat_cnt	'h0d[15:0]	Sets the data latch timing

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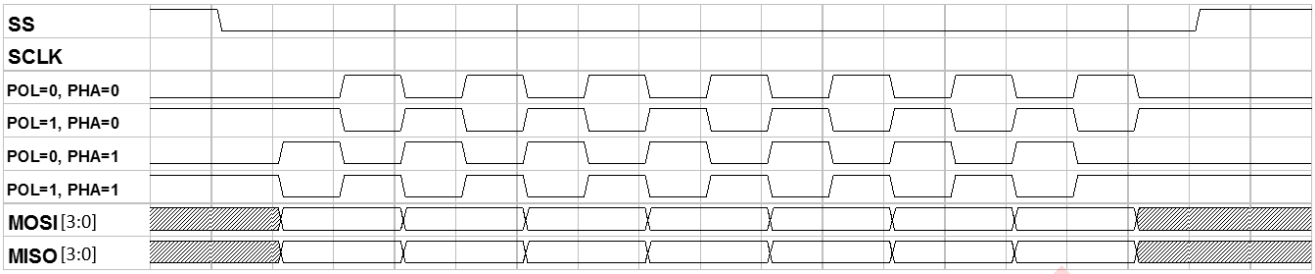
PSPI INTERFACE



POL	PHA	Transfer
0	0	Receive at rising edge, transmit at falling edge
1	0	Receive at falling edge, transmit at rising edge
0	1	Receive at falling edge, transmit at rising edge
1	1	Receive at rising edge, transmit at falling edge

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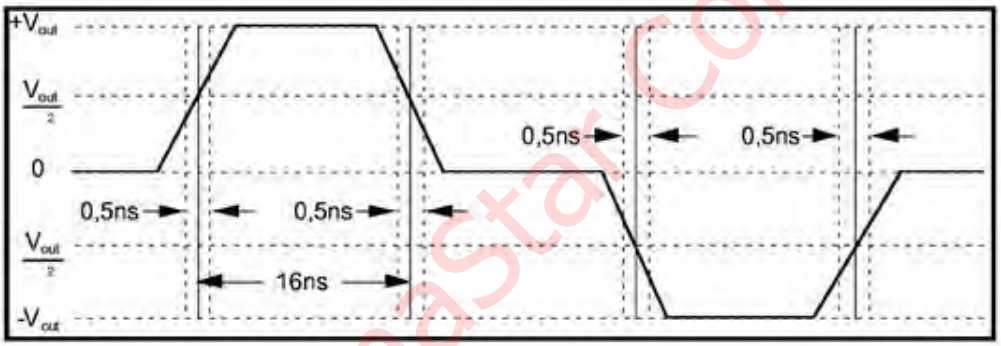
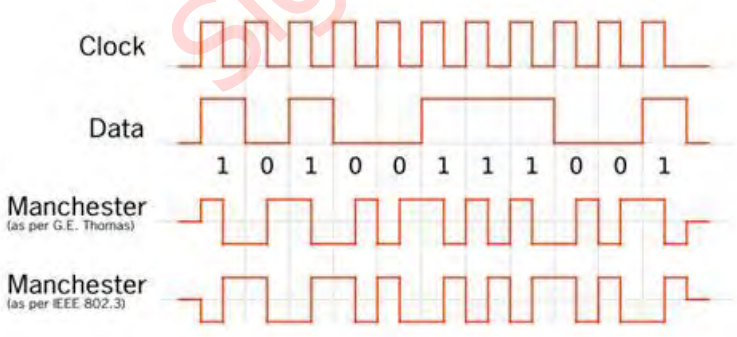
EPHY INTERFACE

Parameter	Min	Typ	Max	Unit
ETHERNET ANALOG INTERFACE (10BASE-T)				
Analog Input Range	4.4	5	5.6	Vdp-p
Differential Input Impedance		100		ohm
ETHERNET ANALOG INTERFACE (100BASE-TX)				
Analog Input Range	1.9	2	2.1	Vdp-p
Differential Input Impedance		100		ohm
Rise/Fall Time	3	4	5	ns
Rise/Fall Time Symmetry			0.5	ns
Duty Cycle Distortion	-0.25		0.25	ns
Amplitude Symmetry	98	100	102	%
Overshoot			5	%

100BASE-TX



10BASE-T



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THERMAL SIMULATION MODE

1. PCB conditions (JEDEC JESD51-5)
2. PCB layers: 2L (1S1P)
3. PCB dimensions (mm x mm): 76.2 x 114.3
4. PCB thickness (mm): 1.6

PKG Type	PKG Size (mm) / Pin Count	PCB Layer	Theta jc (C/W)	Theta jb (C/W)	Ta (C)	Tj (C)	Theta ja (C/W) 0 m/s
QFN	7x7 / 68L	2L	10.61	12.63	70	125	26.75

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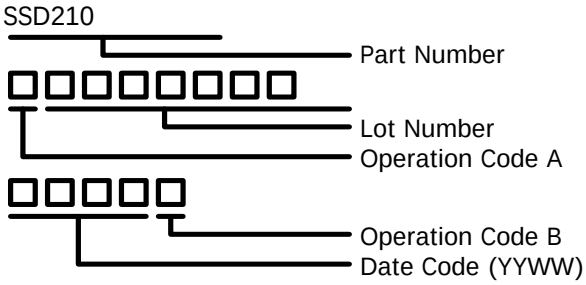
ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option	Minimum Order Quantity
SSD210	-20°C to +85°C	QFN	68-pin	3328ea

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. SSD210 comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

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