SSW102B
Single-chip IEEE 802.11b/g/n 1T1R Wireless Network Controller with SDIO Interface

Data Sheet Version 1.0

REVISION HISTORY

Revision No.	Description	Date
1.0	• Initial release	08/22/2019

1. OVERVIEW

1.1. General Description

SSW102B is a highly integrated 802.11/b/g/n WLAN SOC with SDIO interface (SDIO2.0 compliant). SSW102B provides a complete solution for wireless LAN application with remarkable performance and stability.
SSW102B supports all data rates of IEEE 802.11b, 802.11g, and 802.11n. Features includes one spatial stream transmission, short guard interval (400ns GI), and transmission over 20MHz and 40MHz bandwidth.
SSW102B WLAN MAC supports 802.11e for multimedia applications, 802.11i security, and 802.11n for enhanced MAC protocol efficiency. Frame aggregation techniques such as A-MPDU are also supported for improving throughput performance. Power saving mechanisms such as Legacy Power Save, and U-APSD are implemented to reduce power consumption.
SSW102B is fully compatible with WiFi- Alliance, WMM, WPS and P2P specifications.

1.2. Block Diagram

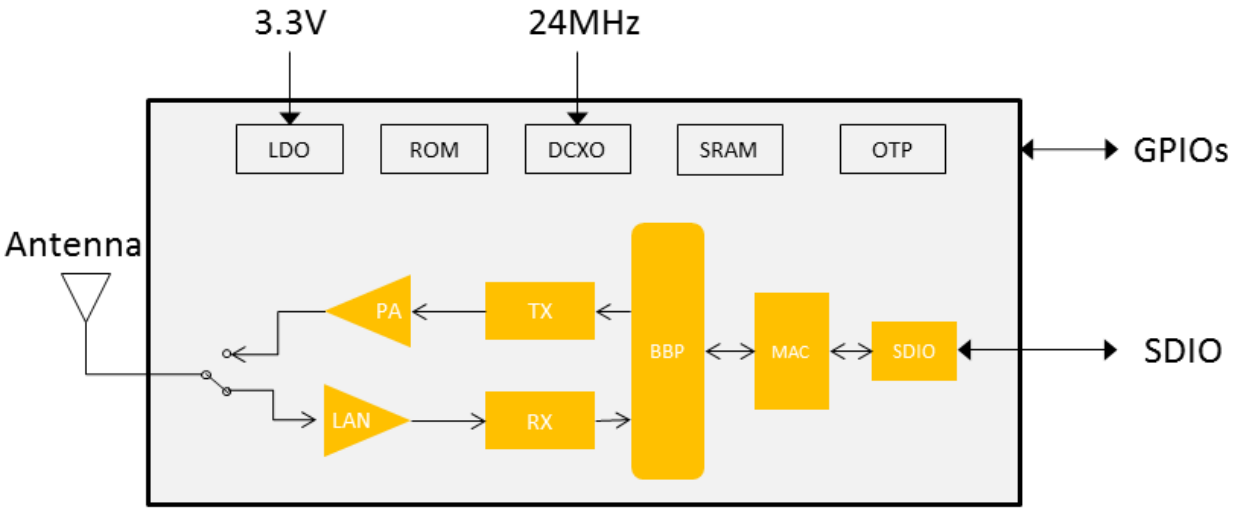

Figure 1: SSW102B Block Diagram

1.3. SSW102B Feature List

- Integrated WLAN MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip
- SSW102B includes Wi-Fi protocol accelerator, SDIO device interface, peripheral interface and Power-Management Subsystem
- Integrated PA, LNA, Balun and T/R switch to minimize BOM cost
- Integrated LDO on chip to simplify power source and reduce BOM cost, only 3.3V power is needed.
- Support BSS, P2P and Miracast function
- Compatible with 802.11 b/g/e/i/n/w specifications
- Compatible with 802.11n Legacy mode, mixed mode and green field mode
- Support A-MPDU transmit and receive for throughput improvement
- Support STA and AP function
- Support A-MSDU reception
- Support STBC stream reception
- Support Short-GI of 802.11n
- Support both 20MHz and 40MHz bandwidth transmission
- PS-Poll and U-APSD Power Save supported at BSS
- Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for radio frequency front-end
- Hardware Crypto Engine for Advanced Fast Security, Including WEP, TKIP, AES and 802.11w
- SDIO device interface with speed up to 200Mbps (SDIO2.0 compliant)
- I2C master/slave, UART, SPI master, PWM and GPIO interface
- Support 24.0MHz crystal as default with internal oscillator, 40.0MHz crystal is also optional
- 32bit CPU core with speed up to 160MHz
- 32.768kHz on-chip crystal
- 4x4mm^2, 28pin QFN package

2. PIN INFORMATION

2.1. Pin Map

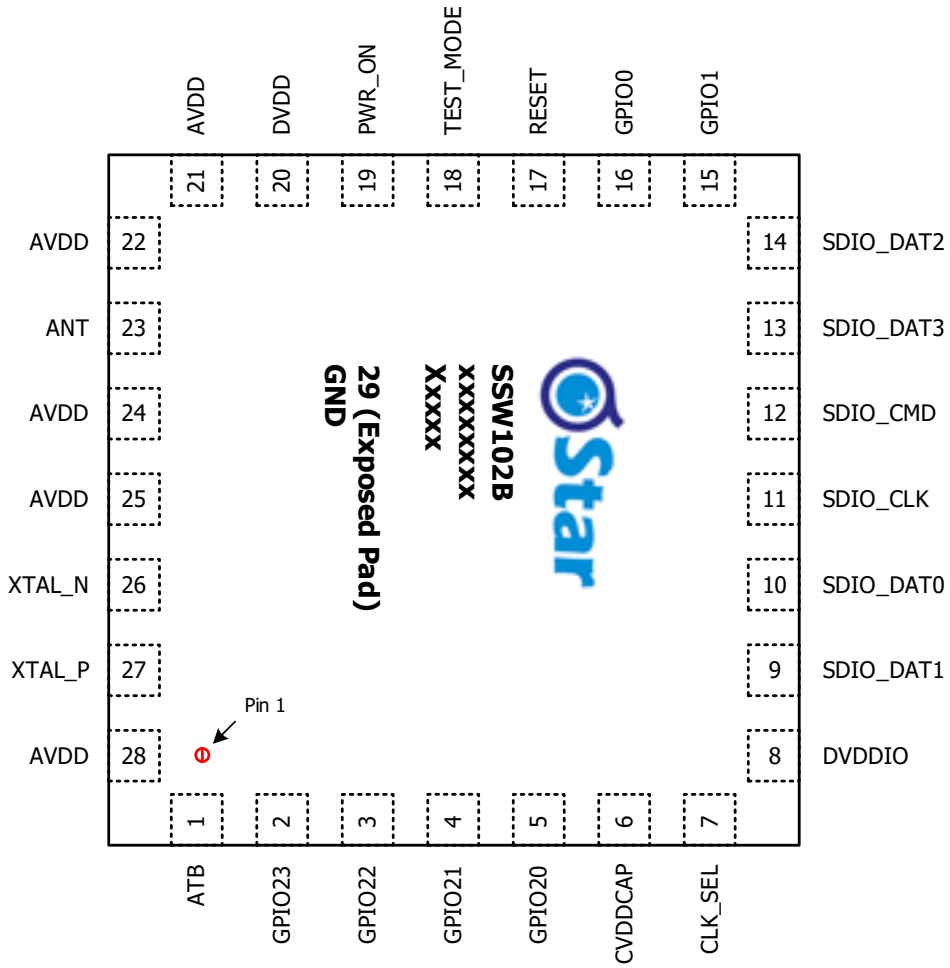

Figure 2: SSW102B Pin Map (Top View)

2.2. Pin Table

Pin Number	Pin Name	Number of Pin(s)	Type	Pin Description
SDIO interface				
14	SDIO_DAT2	1	I/O	SDIO interface data2
13	SDIO_DAT3	1	I/O	SDIO interface data3
12	SDIO_CMD	1	I/O	SDIO interface command
11	SDIO_CLK	1	I/O	SDIO interface clock
10	SDIO_DAT0	1	I/O	SDIO interface data0
9	SDIO_DAT1	1	I/O	SDIO interface data1
Power supply				
6	CVDDCAP	1	PWR	VDD 1.1V for digital core. It is only connected with decouple capacitance. Digital core power is supplied by LDO on chip to reduce power source for BOM cost reduction.
8	DVDDIO	1	PWR	VDD 3.3V or 1.8V, depends on SDIO interface voltage.
20	DVDD	1	PWR	VDD 3.3V or 1.8V for digital circuit, should use same voltage as DVDDIO.
21	AVDD	1	PWR	VDD 3.3V for analog circuit
22	ADDD	1	PWR	VDD 3.3V for analog circuit
24	AVDD	1	PWR	VDD 3.3V for analog circuit
25	AVDD	1	PWR	VDD 3.3V for analog circuit
28	AVDD	1	PWR	VDD 3.3V for analog circuit
GPIO				
2	GPIO23	1	I/O	UART#2 RTS/; SPI#2 CS/; I2C#2 SCL; GPIO; PWM; WLAN_IRQ
3	GPIO22	1	I/O	UART#2 CTS/; SPI#2 MOSI; I2C#2 SDA; GPIO; PWM
4	GPIO21	1	I/O	UART#2 TXD; SPI#2 MISO; GPIO; PWM
5	GPIO20	1	I/O	UART#2 RXD; SPI#2 CLK; GPIO; PWM
15	GPIO1	1	I/O	UART#1 TXD; I2C#1 SCL; SDIO WLAN_IRQ, GPIO; PWM
16	GPIO0	1	I/O	UART#1 RXD; I2C#1 SDA; GPIO; PWM
Reset				
17	RESET	1	Input	Hardware reset pin, low active
19	PWR_ON	1	Input	Power enable pin, low level is chip power down

Test				
1	ATB	1	Output	Analog circuit test pin
18	TEST_MODE	1	Input	Test mode selection, left it floating in normal mode.
Clock				
7	CLK_SEL	1	Input	If uses 24MHz crystal, left it floating
26	XTAL_N	1	Output	Oscillator output
Antenna Interface				
23	ANT	1	I/O	2.4GHz radio signal input/output from/to antenna
GND				
29 (Exposed Pad)	GND	1	GND	Ground for power supplies
27	XTAL_P	1	Input	Oscillator input

3. ELECTRICAL CHARACTERISTICS

3.1. Absolute Maximum Rating

Parameter	Description	Min	Max	Unit
AVDD	Analog circuit 3.3V power supplies voltage	-0.3	5.0	V
DVDD DVDDIO	Digital circuit and digital I/O 3.3V or 1.8V power supplies voltage	-0.3	5.0	V
T_{stg}	Storage temperature	-60	150	°C
T_j	Junction temperature		125	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded.

3.2. Thermal Data

Parameter	Description	Value	Unit
T_{oper}	Operating ambient temperature range	-40 ~ +85	°C
R_{thjc}	Junction-case thermal resistance	15.6	°C/W
R_{thja}	Junction-ambient thermal resistance	30.9	°C/W

3.3. DC Electrical Characteristics

Parameter	Description	Min	Typical	Max	Unit
AVDD	Analog module 3.3V operating voltage	2.97	3.3	3.63	V
DVDD	Digital module 3.3V operation voltage	2.97	3.3	3.63	V
	Digital module 1.8V operating voltage	1.62	1.8	1.98	V
DVDDIO	Digital I/O module 3.3V operation voltage	2.97	3.3	3.63	V
	Digital I/O module 1.8V operating voltage	1.62	1.8	1.98	V
V_{IL} V_{IH}	Low level input voltage (I, I/O) High level input voltage (I, I/O)	-0.3 2.0		0.8 3.6	V V
V_{T+} V_{T-}	Schmitt trig Low to High threshold (I, I/O) Schmitt trig High to Low threshold (I, I/O)	1.54 0.95	1.65 1.02	1.74 1.09	V V
V_{OL} V_{OH}	Low level output voltage (O, I/O) High level output voltage (O, I/O)	 2.4		0.4	V V
I_{GPIO}	GPIOs			9.6	mA

Note: Exposure beyond recommended operating conditions may affect device reliability.

3.4. Requirements to Peripheral Circuits

3.4.1 Power Supply Modules

Type	Power Module	Parameter	Requirement	Unit
3.3V only	3.3V power supply	Rated voltage	3.3	V
		Voltage tolerance	≤10	%
		Rated current	≥400	mA
		Ripple	<120	mV
3.3V and 1.8V	3.3V power supply	Rated voltage	3.3	V
		Voltage tolerance	≤10	%
		Rated current	≥300	mA
		Ripple	<120	mV
	1.8V power supply	Rated voltage	1.8	V
		Voltage tolerance	≤10	%
		Rated current	≥100	mA
		Ripple	<120	mV

3.4.2 External Crystal and Peripheral Circuit

If a 24MHz external crystal is used, the required specification of the crystal should be as below:

Parameter	Description	Min	Typ	Max	Unit
Frequency	Nominal frequency		24.0000		MHz
Tolerance	Frequency measured at 25°C±3°C		±10	±20	ppm
ESR	Equivalent series resistance			40	Ω
C_{Load}	Load capacitance	8	15	16	pF
C_{Shunt}	Shunt capacitance		5		pF
DL	Drive level		120		μW
Aging	Aging per year in 10 years		±5		ppm
Temp Drift	Drift of frequency over the operating temperature range			±20	ppm

If a 40MHz external crystal is used, the required specification of the crystal should be as below:

Parameter	Description	Min	Typ	Max	Unit
Frequency	Nominal frequency		40.0000		MHz
Tolerance	Frequency measured at 25°C±3°C		±10	±20	ppm
ESR	Equivalent series resistance			40	Ω
C_{Load}	Load capacitance	8	15	16	pF
C_{Shunt}	Shunt capacitance		5		pF
DL	Drive level		120		μW
Aging	Aging per year in 10 years		±5		ppm
Temp Drift	Drift of frequency over the operating temperature range			±20	ppm

4. PERIPHERAL INTERFACE

4.1. GPIO interface

SSW102B has six GPIO pins, which can be assigned as different functions by registers setting, such as I2C, UART, SPI and PWM. When these pins are used as GPIO, they may be assigned as High/Low voltage level input/output and high impedance. When these GPIO pins are used as GPIO input, High/Low input voltage level on GPIOs can be read by registers to trigger CPU interruption. The I/O mux of GPIO pins is shown in Table 1.

Table 1: GPIO Interface Definition

Pin Number	Pin Name	I2C	UART	SPI	GPIO	PWM
2	GPIO23	I2C#2 SCL	UART#2 RTS/	SPI#2 CS/	Available	Available
3	GPIO22	I2C#2 SDA	UART#2 CTS/	SPI#2 MOSI	Available	Available
4	GPIO21		UART#2 TXD	SPI#2 MISO	Available	Available
5	GPIO20		UART#2 RXD	SPI#2 CLK	Available	Available
15	GPIO1	I2C#1 SCL	UART#1 TXD		Available	Available
16	GPIO0	I2C#1 SDA	UART#1 RXD		Available	Available

4.2. Clock frequency selection

SSW102B uses external 24MHz crystal as default. On the other hand, SSW102B can also use 40MHz crystal and external clock or oscillator clock input from XTAL_P pin, controlled by strapping pin as shown in Table 2. These strapping pins could connect to GND or I/O power supply directly without resistors.

Table 2: Clock Frequency Selection

Clock type	CLK_SEL Pin #7	GPIO22 Pin #3	GPIO23 Pin #2
24MHz crystal (default)	NC (pull-up internally)	Optional	Optional
40MHz crystal	Low	Low	High
24MHz crystal	Low	Low	Low
40MHz external clock or oscillator	Low	High	High
24MHz external clock or oscillator	Low	High	Low

5. INTERFACE TIMING SPECIFICATION

5.1. SDIO interface timing

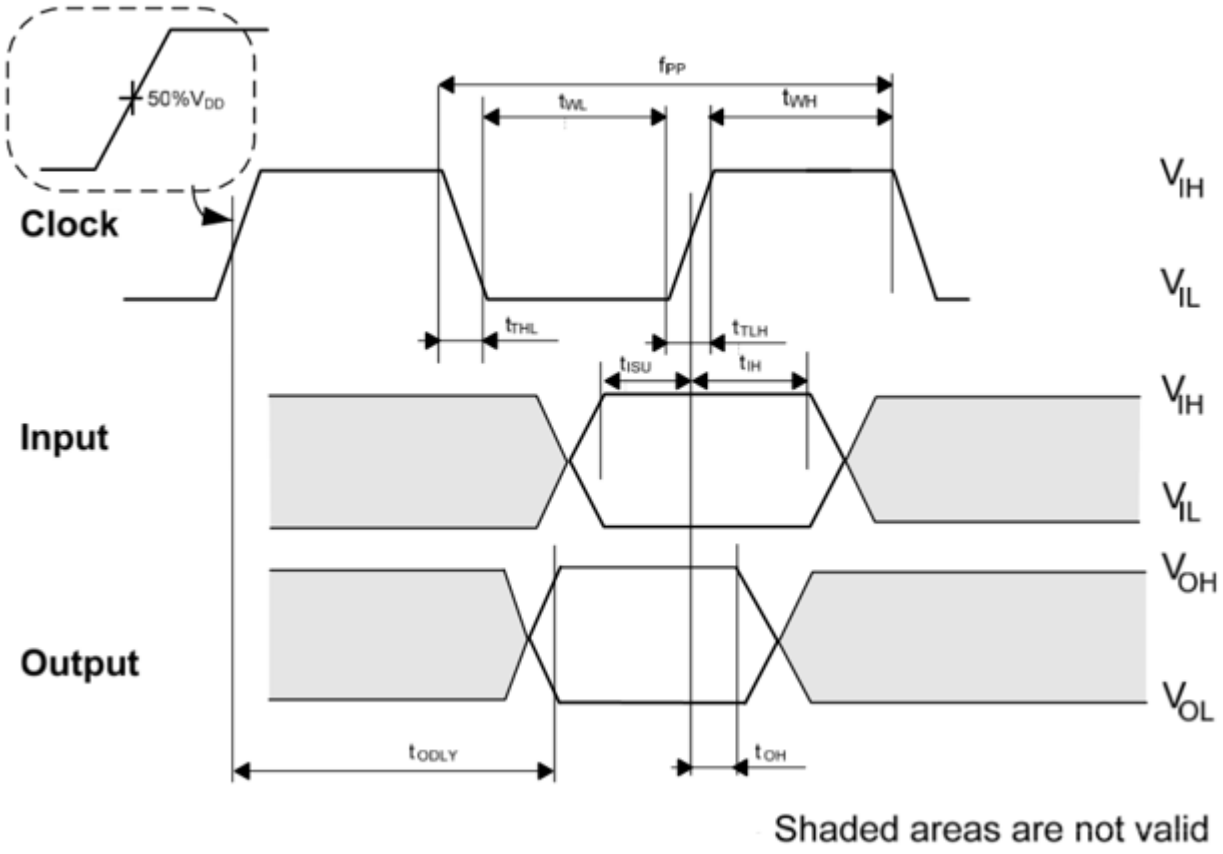

Figure 3: SDIO interface timing

SDIO interface timing requirement is shown as below.

Symbol	Parameter	Min	Typical	Max	Unit
f_{pp}	SDIO clock frequency	0	-	50	MHz
t_{THL}	SDIO clock fall time			3	ns
t_{TLH}	SDIO clock rise time			3	ns
t_{WL}	SDIO clock low time	7			ns
t_{WH}	SDIO clock high time	7			ns
t_{ISU}	Input setup time	6			ns
t_{IH}	Input hold time	2			ns
t_{ODLY}	Output delay time			14	ns
t_{OH}	Output Hold time	2.5			ns

6. MECHANICAL DATA

6.1. Chip Package Drawing

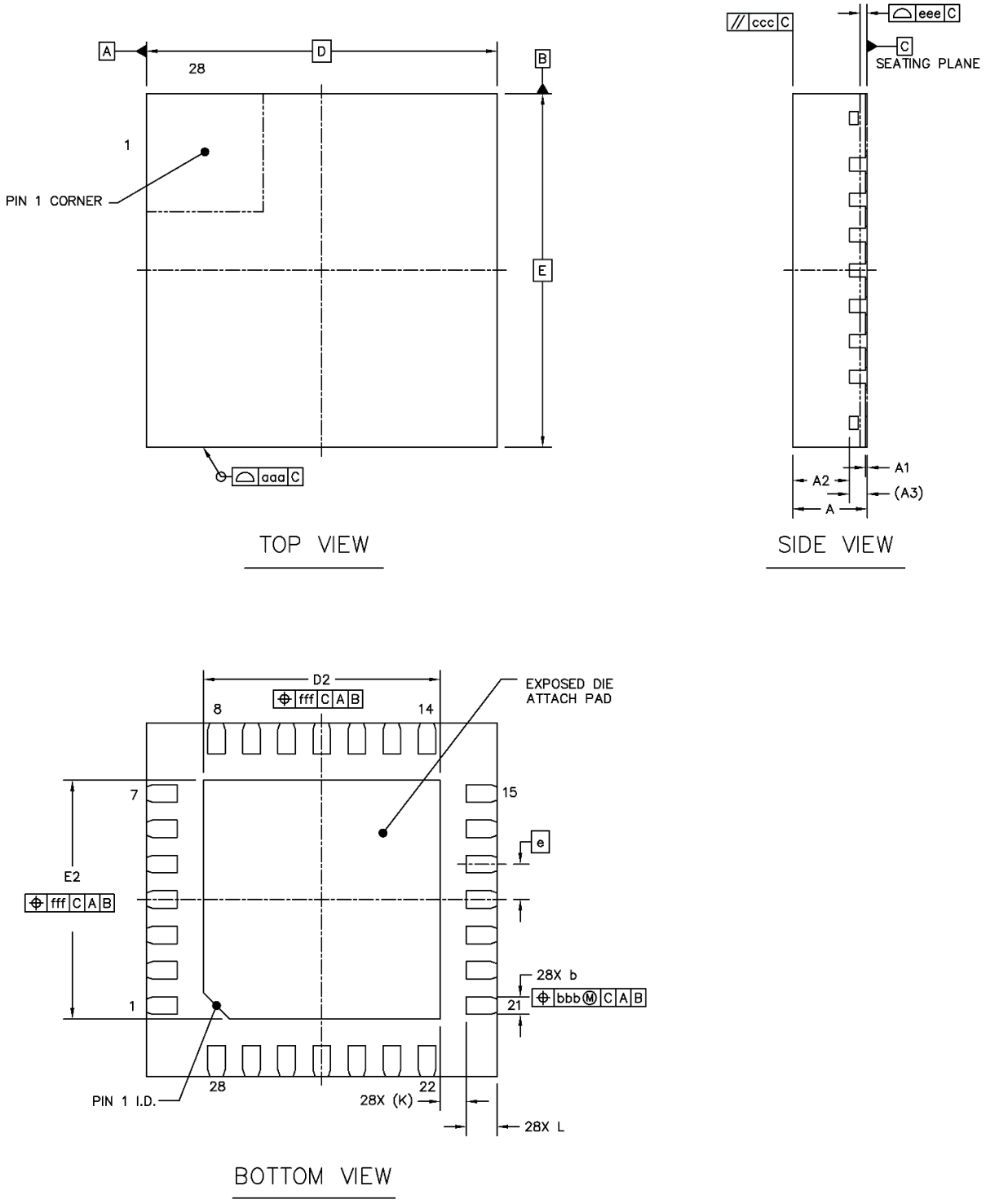

Figure 4: SSW102B Package Drawing

6.2. Dimensions of Packaging Parameters

		SYMBOL	MIM	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.647	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	2.6	2.7	EP SIZE
	Y	E2	2.6	2.7	
LEAD LENGTH		L	0.25	0.35	0.45
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSE PAD OFFSET		fff		0.1	

Unit: mm

7. SOLDER REFLOW PROFILE

7.1. Package Peak Reflow Temperature

SSW102B is assembled in a lead-free QFN28 package. Since its size is 4×4×0.85mm3, the volume and thickness is in the category of volume<350mm3 and thickness<1.6mm in Table 4-2 of IPC/JEDEC J-STD-020C. Accordingly, the peak reflow temperature (Tp) is 260°C.

7.2. Classification Reflow Profile

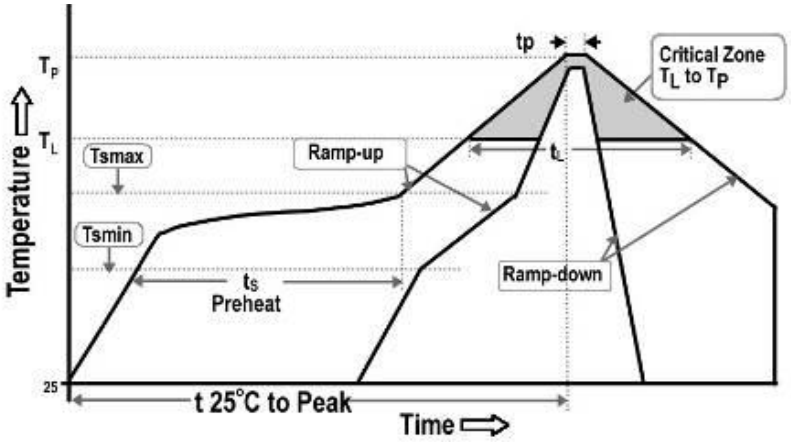

Figure 5: SSW102B Reflow Profile

Profile Feature		Specification*
Average ramp-up rate (t_{smax} to t_P)		3°C/second max.
Pre-heat	Minimal temperature (T_{smin})	150°C
	Maximal temperature (T_{smax})	200°C
	Time (t_s)	60~180 seconds
Time maintained above	Temperature (T_L)	217°C
	Time (t_L)	60~150 seconds
Peak/Classification temperature (T_P)		260°C
Time within 5°C of actual peak temperature (t_P)		20~40 seconds
Ramp-down rate		6°C/second max.
Time 25°C to peak temperature		8 minutes max.

*** Note: all temperatures are measured on the top surface of the package.**

7.3. Maximum Reflow Times

The maximum reflow times are **three (3)** times. All package reliability tests are performed, and passed the tests with a pre-condition procedure that repeats the above reflow profile.